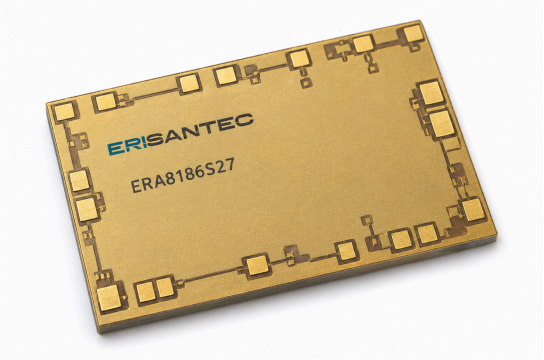
ERA8186S27 | E-band Power Amplifier MMIC

81–86 GHz • Bare die • Engineering datasheet

Key features

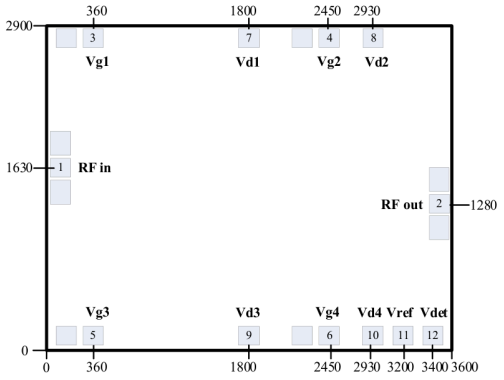
- Frequency range: 81–86 GHz
- Small-signal gain: 18 dB
- Saturated output power: 27 dBm at 13% PAE
- DC supply: Vd = 4 V, Id = 1000 mA (Vg = –0.35 V)
- Die size: 3.60 × 2.90 × 0.07 mm



Product description

ERA8186S27 is an E-band power amplifier die for 81–86 GHz operation. Typical small-signal gain is 18 dB and typical saturated output power is 27 dBm.

Authentic die outline



Dimensions (µm unless noted)

Overall outline tolerance: ±50 µm. Thickness: 70 µm (0.07 mm). All positional dimensions shown in µm.

Electrical characteristics

Vd = 4 V, Id = 1000 mA, TA = +25 °C

Parameter	Min	Typ	Max	Unit
Frequency range	81		86	GHz
Small-signal gain		18		dB
Gain flatness		±1		dB
Saturated output power		27		dBm
Power-added efficiency		13		%
Input VSWR		2		–
Output VSWR		2		–
Saturated drain current		1200		mA

Operating limits

Parameter	Limit
Gate negative voltage	–1.5 V
Drain positive voltage	4.5 V
Input power	20 dBm
Storage temperature	–65 to +150 °C
Operating temperature	–55 to +85 °C

Package technology

Unpackaged MMIC die; wire-bond contacts. Contact geometry is defined by the source drawing.

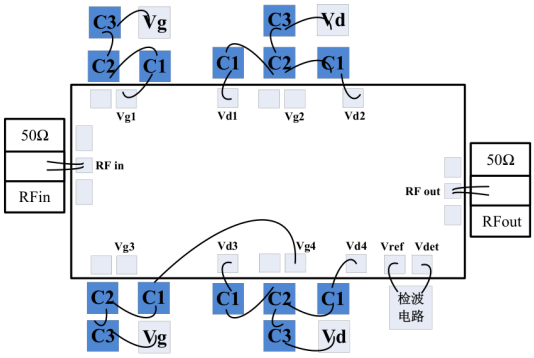
ERA8186S27 | Bond pads and assembly

Contact identification • Recommended external bypass components

Bond-pad definitions

Pin(s)	Symbol	Function / connection	Pad size (µm²)
1	RFin	RF input; external 50 Ω system; no DC-blocking capacitor required.	80 × 80
2	RFout	RF output; external 50 Ω system; no DC-blocking capacitor required.	80 × 80
3, 4 / 5, 6	Vg1, Vg2 / Vg3, Vg4	Gate bias pads; external 100 pF, 10000 pF and 10 µF bypass capacitors.	100 × 100
7, 8 / 9, 10	Vd1, Vd2 / Vd3, Vd4	Drain bias pads; external 100 pF, 10000 pF and 10 µF bypass capacitors.	100 × 100
11, 12	Vref, Vdet	Detector reference and detector output; connect to an external detection circuit.	100 × 100

Recommended assembly layout



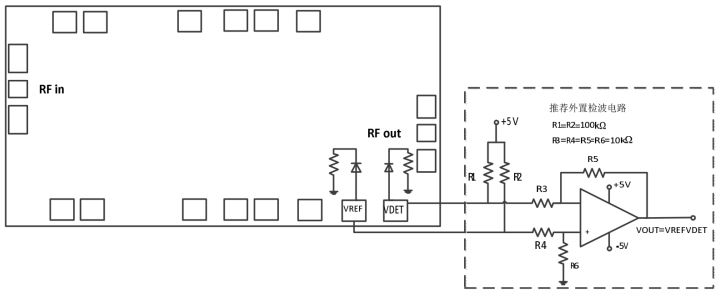
Bypass components

C1 = 100 pF; C2 = 10000 pF; C3 = 10 µF. Use a single-layer capacitor for C1 where possible, installed as close as possible to the die bond pad.

Vg1 and Vg3 share one bias feed; Vg2 and Vg4 share one bias feed.

Recommended detector circuit

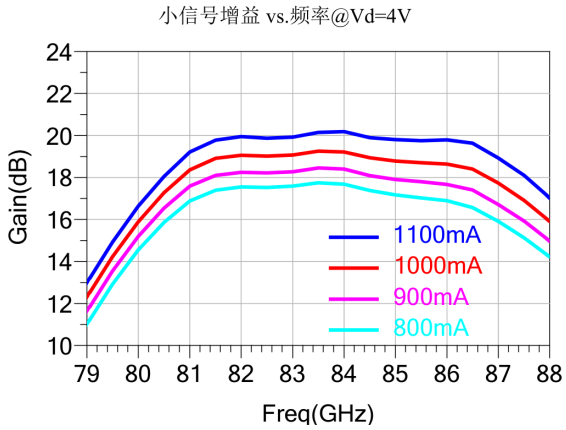
Original detector schematic (Vref / Vdet).



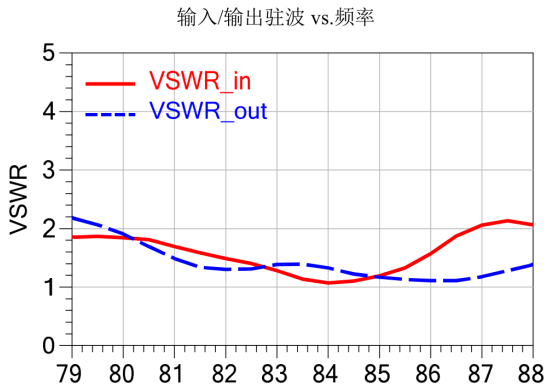
ERA8186S27 | RF performance plots

On-wafer pulsed tests at TA = +25 °C; Vd = 4 V, Id = 1000 mA

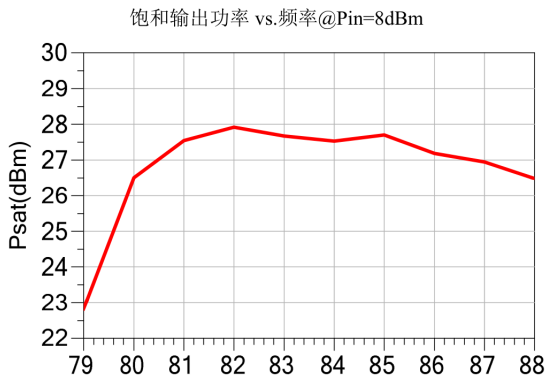
Small-signal gain vs. frequency



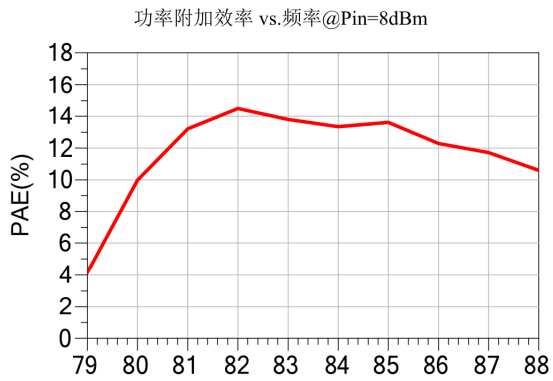
Input / output VSWR vs. frequency



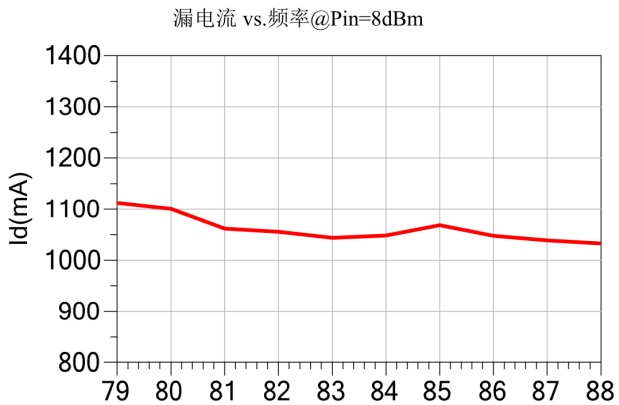
Saturated Pout vs. frequency (Pin = 8 dBm)



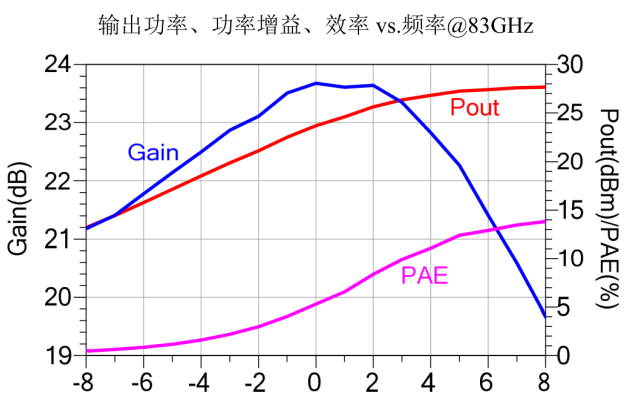
PAE vs. frequency (Pin = 8 dBm)



Drain current vs. frequency (Pin = 8 dBm)



Power, gain and PAE vs. Pin at 83 GHz



ERA8186S27 | Handling and installation

Source engineering precautions • Bare semiconductor MMIC

Handling and safety requirements

01 Storage

Keep the die in an ESD-protected container and store in a nitrogen atmosphere.

02 Cleaning

Handle bare die in a clean environment. Do not use liquid cleaning agents.

03 ESD protection

Strictly observe ESD handling procedures to avoid electrostatic damage.

04 Handling tools

Use a vacuum pick-up tool or precision pointed tweezers; do not touch the die surface with fingers or tools.

05 Bias sequence

At power-up, apply gate voltage before drain voltage. At power-down, remove drain voltage before gate voltage.

06 Die attachment

Use AuSn eutectic soldering or conductive adhesive. The mounting face must be flat and clean and the RF substrate gap minimized. For 80/20 AuSn, keep sintering temperature below 300 °C, duration at or below 20 s and scrubbing time at or below 3 s. For conductive adhesive, apply as little as possible and follow the adhesive vendor cure conditions.

07 Wire bonding

Unless otherwise stated, use two 25 µm-diameter gold wires for each RF input and output bond. Keep bond wires as short as possible.

08 Support

Contact the supplier if there are technical questions.

Source notation

All numeric limits, bias sequencing and bonding constraints follow the original supplier datasheet. Charts and engineering drawings are preserved from the source.