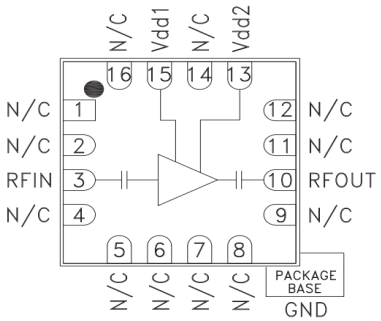
ER451SP3E

GaAs MMIC Driver amplifier chip 5-20GHz

Performance Features:

- Frequency band: 5~20GHz
- Gain: 23dB
- Output P1dB: 18.5dBm
- Saturated output power: 20dBm
- Output IP3:32dBm
- Input/output return loss: 18dB/11dB
- Power supply: +5V@105mA
- Package size: 3×3mm

Functional Diagram



Product Description:

ER451SP3E a GaAs MMIC driver amplifier chip with a frequency range covering 5~20GHz and an output P1dB of 18.5dBm over the entire band.

Electrical parameters:(T_A=25℃, VD=+5V)

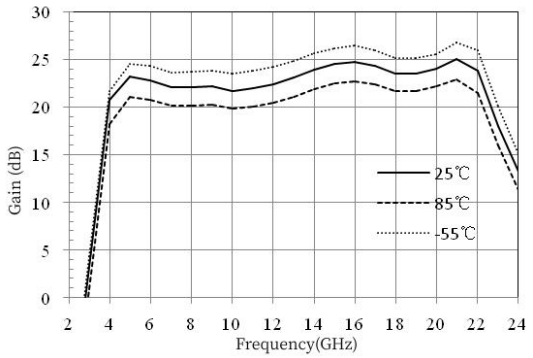
Index	Minimum	Typical value	Maximum value	Units
Frequency range	5~20			GHz
Gain	22	23	25	dB
Output P1dB	18.5	-	-	dBm
Saturated output power	20	-	-	dBm
Output IP3	32	-	-	dBm
Input return loss	-	18	-	dB
Output return loss	-	11	-	dB

Use limit parameters: (Exceeding any of the above maximum limits risks permanent damage.)

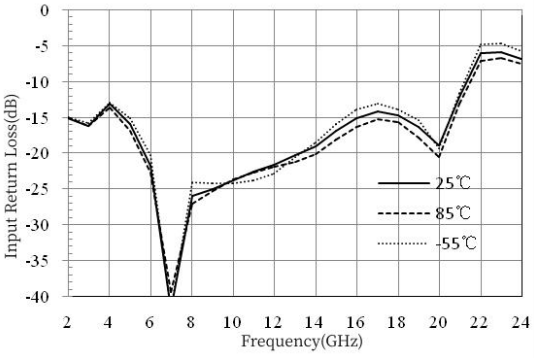
Input power	+10dBm
Voltage	+6V
Storage temperature	-65℃~150℃
Service temperature	-55℃~125℃

Typical curve:

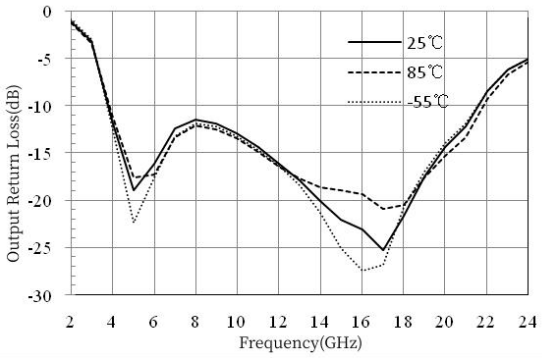
Gain Vs temperature



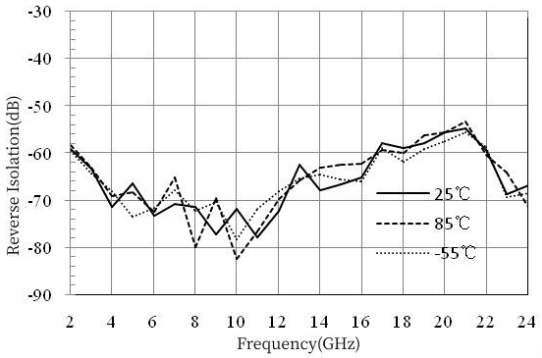
input return loss Vs temperature



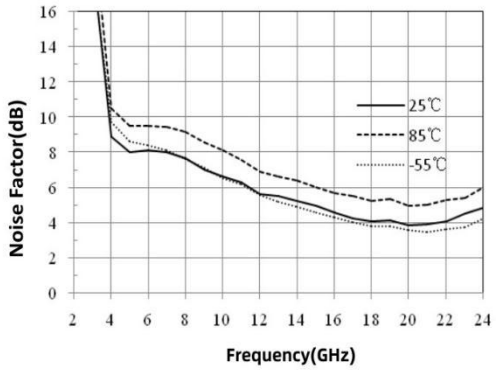
Output return loss Vs temperature



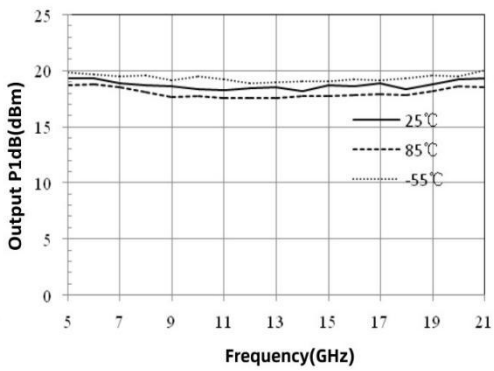
reverse isolation Vs temperature



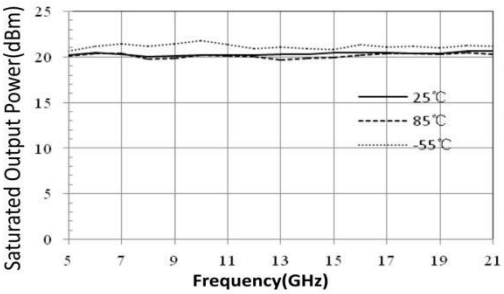
Noise factor Vs temperature



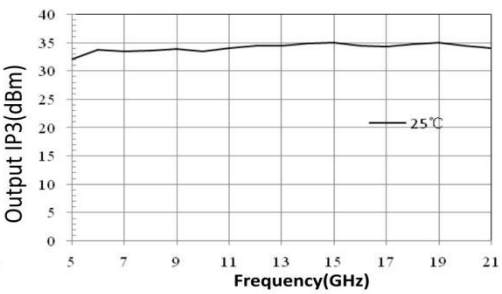
Output P1dB Vs temperature



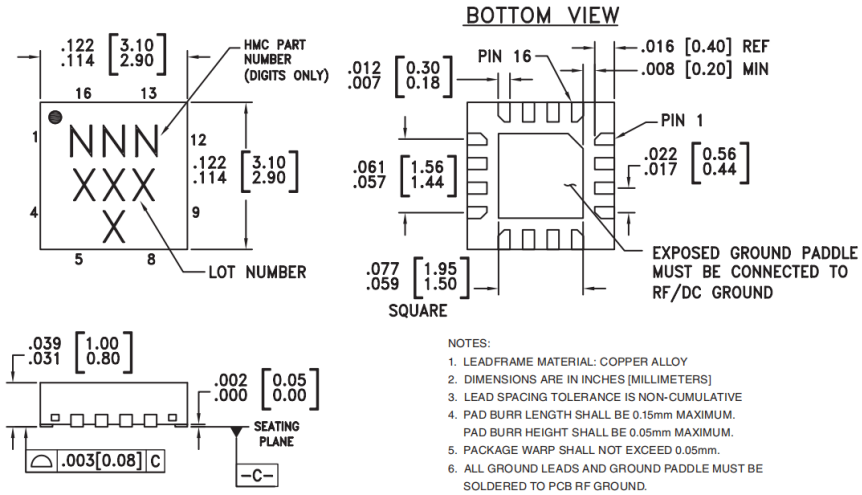
Saturated output power Vs temperature



Output IP3（25℃）



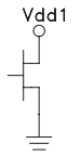
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 4 - 9, 11, 12, 14, 16	N/C	This pin may be connected to RF/DC ground. Performance will not be affected.	
3	RFIN	This pin is AC coupled and matched to 50 Ohms.	
10	RFOUT	This pin is AC coupled and matched to 50 Ohms.	
13	Vdd2	Power Supply Voltage for the amplifier. External bypass capacitors of 100 pF, 1,000 pF and 2.2 µF are required.	
15	Vdd1	Power Supply Voltage for the amplifier. External bypass capacitors of 100 pF, 1,000 pF and 2.2 µF are required.	
	GND	Package bottom must be connected to RF/DC ground.	

Instructions:

Note: I/O has straight capacitance

Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.

Cleaning treatment: The bare chip must be operated and used in a purified environment. It is forbidden to use liquid cleaning agent to clean the chip.

Electrostatic protection: Strictly comply with the ESD protection requirements to avoid electrostatic damage to the components.

General operation: Use vacuum chuck or precision pointed tweezers to pick up the chip.Avoid touching the surface of the chip with tools or fingers during handling.

Mounting operation: The chip can be installed using AuSn solder eutectic welding or conductive adhesive bonding process.The mounting surface must be clean and flat.

Bonding operation: Input and output with 2 (recommended diameter of 25um gold wire) bonding wire, bonding wire length less than 250um is optimal.It is recommended to use the smallest possible ultrasonic energy.Bonding begins at the pressure point on the chip and ends at the package (or substrate).